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EXAMINER	
NGUYEN, VAN THU T	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 04/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/974,962	Applicant(s) TAKAHASHI ET AL.	
	Examiner VanThu Nguyen	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment A* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-9 and 13-18* is/are allowed.

6)☒ Claim(s) *1-3,10-12,19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search Report* .

Response to Amendment

1. Amendment A filed on March 26, 2003 has been entered.

2. Claims 1-19 are still pending.

Priority

3. Applicant is reminded that in order for a patent issuing on the instant application to obtain the benefit of priority based on priority papers filed in parent Application No. 08/574,104 under 35 U.S.C. 119(a)-(d) or (f), a claim for such foreign priority must be made in this application. In making such claim, applicant may simply identify the application containing the priority papers.

Office Action Paper #7 has mistakenly stated that foreign certified copy of the priority document Japan 06-334950 filed on December 20, 2994 has been received in Application No. 08/574,104. However, there is no statement from Applicant to identify which application containing this priority paper.

Response to Arguments

4. Applicant's arguments with respect to claims 1, 10, 19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 10-12, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. Patent No. 6,307,217) in view of Sawada et al. (U.S. Patent No. 5,471,430).

Regarding claim 1, Ikeda et al. disclose a semiconductor memory comprising:

a plurality of first regions arranged in lattice fashion (SMA, see FIG. 2), each of which corresponds to a memory array including a plurality of main word lines (MWL, see FIG. 2) extending in a first direction (horizontal), a plurality of sets of sub-word lines (SWL, see FIG. 3) extending in said first direction, a plurality of pairs of data lines (complementary data lines DLs, see FIG. 3) extending in a second direction (vertical) perpendicular to said first direction and a plurality of memory cells, each of which is coupled to a corresponding one of said plurality of sub-word lines and a corresponding one of said data lines, one of said plurality of main word lines being allotted to one of said plurality of sets of sub-word lines (see column 11 lines 1-23);

a plurality of second regions (WDEC, see FIG. 3), each of which is arranged alternately with each of said first regions arranged along said first direction and each of which includes sub-word line drivers connected to said sub-word lines (a WDEC is located at one end of each of SMA, see column 11, lines 1-2).

a plurality of third regions (YSW, YDEC, SA, see FIG. 3), each of which is arranged alternately with each of said first regions arranged along said second direction and each of which includes sense amplifiers (SA, see FIG. 3) connected to said data lines; and

a plurality of fourth regions (regions between where DATA BUS running across, see FIG. 3), each of which is arranged alternately with each of said third regions arranged

along said first direction, wherein each of said plurality of main word lines extends through one or more of said first regions arranged along said first direction;

wherein said semiconductor memory further includes:

a plurality of pairs of sub-common data lines (vertical output lines from SA, see FIG. 3).

first switching circuits (YSW, see FIG. 3) formed in said third regions and connected interposingly between said plurality of pairs of data lines and a corresponding one of said pairs of sub-common data lines;

a plurality of pairs of main-common data lines (DATA BUS, see FIG. 3); and

second switching circuits (MP, see FIG. 27) formed in said fourth regions and connected interposingly between a corresponding one of said pairs of main-common data lines and a corresponding one of said pairs of sub-common data lines.

However, Ikeda et al do not disclose that each of said pairs of sub-common data lines extends in said first direction through said third regions arrange along said first direction; and each of said pairs of main-common data lines extends in said second direction through one or more of second regions arranged along said second direction.

Sawada et al. disclose, in FIG. 4, a semiconductor memory comprising:

a plurality memory arrays MK which have word lines extend in horizontal direction (so called first direction); and data lines or bit lines extend in vertical direction (so called second direction); said plurality memory arrays MK have alternately arranged shared type sense amplifier structures in vertical;

a plurality of sub-common data lines (LIO1-LIO4), each of which extends in horizontal through the regions of sense amplifiers; first switching circuits (CSG1-CSG2) connecting plurality of pairs of data lines and corresponding one of said pairs of sub-common data lines.

a plurality of main-common data lines (GIO1-GIO2), each of which extends in vertical through the regions adjacent to the memory arrays; second switching circuits (BS1, BS2) connecting corresponding pairs of sub-common data lines with corresponding pairs of main-common data lines.

Since Ikeda et al. and Sawada et al. are both from the same field of semiconductor, the purpose disclosed by Sawada et al. would have been recognized in the pertinent art of Ikeda et al.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to arrange sub-common data lines and main-common data lines in prefer directions because it's only a design choice.

Regarding claims 2-3, Ikeda et al. further disclose a number of memory arrays allotted to one of said main word-lines (which is 32 SMA, see FIG. 2) is greater than a number of memory arrays allotted to a corresponding one of said pairs of sub-common data lines (which is ½ of SMA, see FIG. 3); length of said each main word-line is longer than a length of said each pair of sub-common data lines (observing from FIGS. 2 and 3).

Regarding claims 10-12, they are rejected under U.S.C. 103(a) since they recite similar limitation as in claims 1-3, except replacing plurality pairs of data lines/sub-common data lines/main data lines with plurality of data lines/sub-common data lines/main data lines.

However, "plurality of pairs of data lines/sub-common data lines/main data lines" can also be considered as "plurality of data lines/sub-common data lines/main data lines".

Regarding claim 19, Ikeda et al. in view of Sawada et al. disclose a semiconductor comprising a plurality of word lines layered by main word lines (MWL) and sub-word lines (SWL) (see FIG. 14); a plurality of I/O lines inherently layered by data lines (DLs), sub-common data lines (output from SA) connected to said data lines and main-common data lines (DATA BUS) connected to said sub-common data lines (see FIG. 3)

However, Ikeda et al. does not disclose that sub-common data lines extends in the same direction as main word lines and sub-word lines, and main-common data lines extend in the same direction as data lines.

Sawada disclose, in FIG. 4, sub-common data lines (LIO) extend in the same direction as sub-word lines, and main-common data lines extend in the same direction as data lines.

Since Ikeda et al. and Sawada et al. are both from the same field of semiconductor, the purpose disclosed by Sawada et al. would have been recognized in the pertinent art of Ikeda et al.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to arrange sub-common data lines and main-common data lines prefer directions because it's only a design choice.

Allowable Subject Matter

7. Claims 4-9, 13-18 are allowed.

The following is a statement of reasons for the indication of allowance:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Ikeda et al. and Sawada et al. taken individually or

in combination, do not teach the claimed invention having first region, second region, third region, fourth region, fifth region being arranged as in claims 4, 7, 13, 16.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (703) 306-9121. The examiner can normally be reached on Monday-Thursday, 7:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (703) 308-2816. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VTN
April 25, 2003

Van Thu Nguyen

VAN THU NGUYEN
PATENT EXAMINER